What is claimed is:

[Claim 1] 1. A wafer level chip scale package structure process, comprising:

providing a glass substrate having a first surface and a second surface, wherein an interconnect pattern is disposed on the first surface of the glass substrate;

providing a wafer comprising a plurality of chips and having an active surface and a back surface, wherein a plurality of bumps is disposed on the active surface of the wafer;

flipping the wafer, so that the active surface of the wafer faces the first surface of the glass substrate;

disposing the wafer on the glass substrate and connecting the active surface of the wafer to the first surface of the glass substrate through attachment of the bumps and the interconnect pattern;

dicing the wafer;

drilling the glass substrate to form a plurality of through holes; and

forming a plurality of via plugs in the through holes in the glass substrate;

dicing the glass substrate and the interconnect pattern to form a plurality of chip scale package structures.

[Claim 2] 2. The process of claim 1, wherein the glass substrate is an indium tin oxide glass plate.

[Claim 3] 3. The process of claim 1, wherein the bumps are attached to the interconnection pattern of the substrate by eutectic bonding.

[Claim 4] 4. The process of claim 1, wherein the bumps are attached to the interconnection pattern of the substrate by using anisotropic conductive film (ACF).

[Claim 5] 5. The process of claim 1, wherein a redistribution layer is formed on the second surface of the glass substrate and a plurality of solder balls are formed on the second surface of the glass substrate, after dicing the glass substrate and the interconnect pattern.

[Claim 6] 6. The process of claim 1, wherein a wafer level testing process is performed through the via plugs or the interconnect pattern before dicing the glass substrate and the interconnect pattern.

[Claim 7] 7. The process of claim 1, wherein the via plugs are formed by plating.

[Claim 8] 8. The process of claim 1, wherein a material of the via plug is copper.

[Claim 9] 9. The process of claim 1, further comprising grinding the wafer from the back surface of the wafer before dicing the wafer.

[Claim 10] 10. A wafer level chip scale package structure process, comprising:

providing a glass substrate having a first surface and a second surface;
providing a wafer comprising a plurality of chips that are to be separated along scribe-lines and having an active surface and a back surface, wherein a plurality of pads are disposed on the active surface of the wafer and cover a portion of the scribe-lines of the wafer;
flipping the wafer in order to face the active surface of the wafer to the first surface of the glass substrate and attaching the active surface of the wafer to the first surface of the glass substrate;
drilling the glass substrate to form a plurality of through holes and forming a plurality of via plugs in the through holes in the glass substrate; and
dicing the wafer and the glass substrate along the scribe-lines to form a plurality of chip scale package structures.

[Claim 11] 11. The process of claim 10, wherein the glass substrate has no interconnection pattern.

[Claim 12] 12. The process of claim 10, wherein the pads are attached to the glass substrate through a thermal cured adhesive.

[Claim 13] 13. The process of claim 10, wherein a redistribution layer is formed on the second surface of the glass substrate and a plurality of solder balls are formed on the second surface of the glass substrate, after dicing the wafer and the glass substrate.

[Claim 14] 14. The process of claim 10, wherein a wafer level testing process is performed through the via plugs before dicing the wafer and the glass substrate.

[Claim 15] 15. The process of claim 10, further comprising removing the scribe-lines of the wafer from the second surface of the wafer by etching.

[Claim 16] 16. The process of claim 10, further comprising grinding the wafer from the back surface of the wafer, after attaching the active surface of the wafer to the first surface of the glass substrate.

[Claim 17] 17. The process of claim 10, wherein the via plugs are formed by plating.

[Claim 18] 18. The process of claim 10, wherein a material of the via plug is copper.

[Claim 19] 19. The process of claim 10, wherein each of the via plugs is aligned to and connected to one pad.